Pulse Discharge Characteristics of Surface Mount Capacitors

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Abstract

ARC Technology is developing pulse generators for extremely compact geometries requiring megawatts of power and milliJoule to Joule of total energy. These devices are to be constructed with surface mount components and circuit board fabrication techniques to minimize volume, cost, and production time. Clearly, the components in these circuits are operating well beyond their design specifications.

Therefore, this paper examines the energy storage and peak power capabilities of various surface mount capacitor technologies and vendors to determine their applicability in miniature pulsed power circuits.

I. Introduction

ARC Technology is investigating surface mount ceramic capacitors for high current, low voltage applications. Capacitors were studied over the range of 250 V to 1000 V and 0.1 μF to 0.5 μF, with Type II X7R ceramics for high energy density. This paper presents the performance of a representative sample of capacitors from this study, using a simple Spice model to quickly select the best candidates for detailed analysis.

Communication with capacitor manufacturers demonstrated that detailed Spice models are not available for high voltage, high capacitance surface mount technology (SMT) devices over approximately 100 V. Therefore, a first-pass circuit model with an inductor, resistor, and capacitor in series (LRC) was developed to calculate parasitic values for the capacitors from their current waveforms during pulse discharge, with emphasis on predicting the risetime and peak current. These values are verified in Spice and then used to derive the energy and peak power densities of each capacitor.

It should be noted that the results of this study specifically target single shot applications where risetime and peak current are critical, but the subsequent tail of the pulse is not of interest. Therefore, the derived model reasonably predicts the risetime and peak power of the capacitor discharge while the voltage is still relatively high. However, the model does not match the tail characteristics, which include strong effects from the nonlinear capacitance of X7R with respect to voltage.

II. Experimental arrangement

Characterization of a significant number of surface mount capacitors requires the development of rapid testing techniques. The test arrangement shown in Fig. 1 measures the capacitor's pulse discharge characteristics with a minimum of inductance. The current viewing resistor (CVR) must have a resistance that is approximately less than or equal to the associated SMT capacitor impedance. The CVR chosen is a Caddock CC2015FC surface mount 0.020 Ω high current device, which is soldered directly across the voltage monitoring SMA connector. The capacitor under test is soldered on one end to the ground terminal of the SMA connector and in parallel with the CVR. The high voltage power supply is connected through two isolation resistors to the ground side of the SMA connector and to the remaining capacitor terminal.

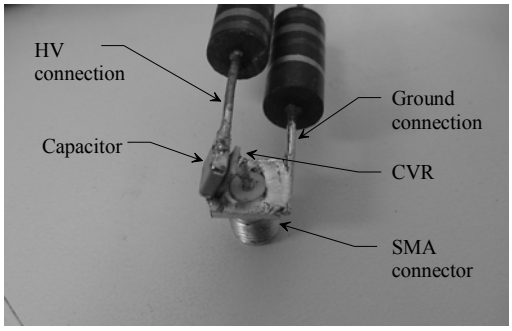

Fig. 1. Test bed configuration.

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Each capacitor in turn is soldered into the test apparatus and charged to its rated voltage. The pulse discharge is initiated by shorting the capacitor high voltage terminal directly to the center pin of the SMA. The resulting transient event is measured with a Tektronix TDS694C Digital Real-Time Oscilloscope. This arrangement provides consistent measurements with variations in the measured peak amplitudes and risetimes of only a few percent.

III. Experimental results

A wide range of high capacitance SMT capacitors have been tested for use in pulse discharge circuits. However, the available capacitance values and rated voltages varied considerably between vendors. Measured waveforms for six representative SMT capacitor pulse discharges are depicted in Fig. 2.

IV. Simulation model development

Initially it was anticipated that the capacitor study would compare models for various high voltage SMT packages to down-select several viable candidates for in-depth testing. However, communication with various high voltage SMT capacitor manufacturers revealed that extensive Spice models do not exist for high voltage, high capacitance SMT devices because they are typically used in bypass and filter circuits.

Therefore, a simple LRC circuit model was developed based on the current waveform from the pulse discharge waveforms of Fig. 2. An approximate solution of the equation for current is derived in terms of the peak amplitude and its associated time. Assuming the capacitance is constant at its nominal value, a solution for R and L is established. These parameters are then compared with measured values to determine the SMT device values.

Both the underdamped and overdamped cases are considered, with critical damping being a special case of each. The underdamped solution is derived in detail. The overdamped solution is mathematically similar except for the use of hyperbolic functions.

A. Underdamped LRC Circuit

$$\tau = \frac{L}{R} \tag{1}$$

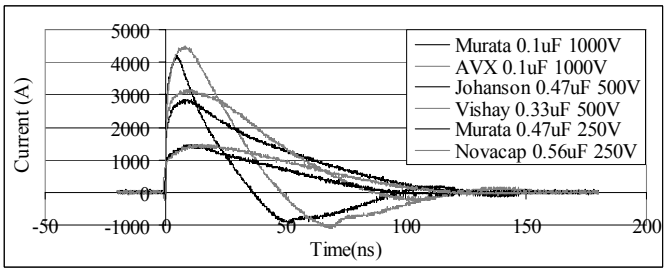

Fig. 2. Discharge measurements for various SMT capacitors.

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{1}{2\tau}\right)^2} \tag{2}$$

$$I(t) = \frac{V}{L\omega} e^{-\frac{t}{2\tau}} \sin(\omega t) \tag{3}$$

$$\frac{dI(t)}{dt} = -\frac{V}{L\omega} e^{-\frac{t}{2\tau}} \sin(\omega t) + \frac{V}{L} e^{-\frac{t}{2\tau}} \cos(\omega t) \tag{4}$$

At peak current:

$$\frac{dI(t)}{dt} = 0 \tag{5}$$

$$\frac{1}{2\tau\omega} \sin(\omega t) = \cos(\omega t) \tag{6}$$

$$2\tau\omega = \tan(\omega t) \tag{7}$$

For the case where $\omega t < 1$

$$\tan(\omega t) \approx \omega t \tag{8}$$

This is valid for the parameters of interest, where L ~ 1 nH, C ~ 100 nF, R ~ fraction of an Ohm, and t ~ several nanoseconds at the current maximum.

Therefore:

$t \approx 2\tau$ at the point of peak current (9)

Substituting (9) back into (3):

$$I_{\max} = \frac{V}{L\omega} e^{-1} \sin(\omega 2\tau) \tag{10}$$

For the case where $\omega 2\tau < 1$

$$\sin(\omega 2\tau) \approx \omega 2\tau \tag{11}$$

This is reasonable for the parameters above and τ ~ ns

Therefore,

$$I_{\max} \approx \frac{V}{eL}(2\tau) \tag{12}$$

From (1) and (12):

$$R = \frac{2V}{eI_{\max}} \tag{13}$$

$$L = \frac{1}{2} R t_{I_{\max}} \tag{14}$$

B. Overdamped LRC Circuit

The overdamped case closely follows the derivation above, with the exception that as the frequency becomes imaginary, ω becomes ϖ and the trigonometric functions become hyperbolic [1].

$$\varpi = \sqrt{\left(\frac{1}{2\tau}\right)^2 - \frac{1}{LC}} \tag{15}$$

Equation (7) then becomes:

$$2\tau\omega = \tanh(\varpi t) \tag{16}$$

For the case where $\varpi t < 1$

$$\tanh(\varpi t) \approx \varpi t \tag{17}$$

which is still valid over the parameters described.

Equation (10) becomes:

$$I_{\max} = \tfrac{V}{L\omega} e^{-1} \sinh(\varpi 2\tau) \tag{18}$$

For the case where $\omega 2\tau < 1$

$$\sinh(\varpi 2\tau) \approx \varpi 2\tau \tag{19}$$

which continues to parallel the underdamped case.

Therefore (13) and (14) are approximate solutions for L and R in both the underdamped and overdamped cases for the parameter range described. These equations describe the circuit variables in terms of the measured peak current and its associated time.

The SMT package parameters are calculated from these values, knowing the resistance of the CVR and assuming that the physical layout of the measurement above is a minimum inductance for the package.

$$R_{capacitor} = R - R_{CVR} \tag{20}$$

$$L_{capacitor} = L \tag{21}$$

The peak current and its associated time are measured for each capacitor from the waveforms in Fig. 2. Then (13), (14), (20), and (21) are used to calculate the capacitor parameters. The results are tabulated in Table 1.

V. Comparison of Results

The calculated parameters of Table 1 are simulated and plotted with their respective measured waveforms in Fig. 3 through Fig. 8. The peak current and peak times are tabulated in Table 2 along with error calculations. The model reasonably predicts the peak current, but is less accurate at predicting the time of the current peak and the risetime.

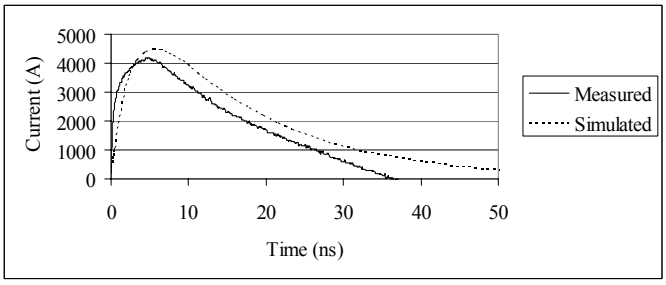

Fig. 3. Murata 0.1 µF, 1000 V measured and simulated current.

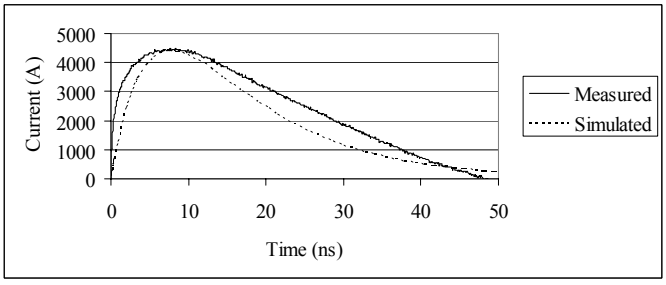

Fig. 4. AVX 0.1 µF, 1000 V measured and simulated current.

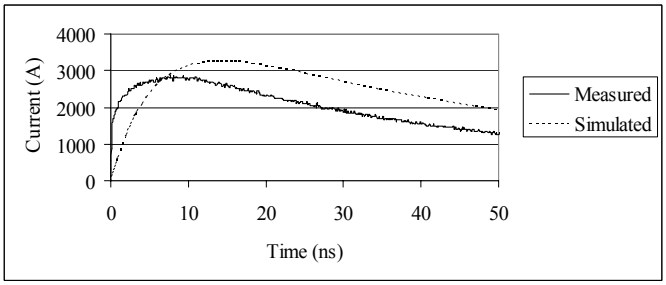

Fig. 5. Johanson 0.47 µF, 500 V measured and simulated current.

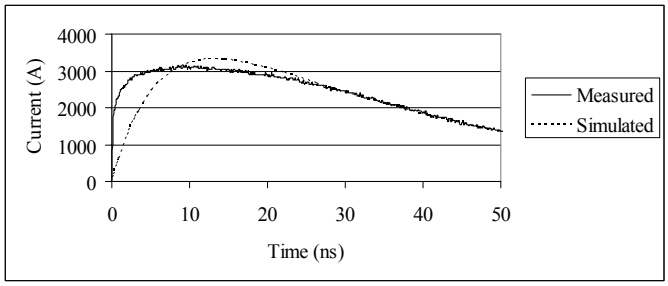

Fig. 6. Vishay 0.33 µF, 500 V measured and simulated current.

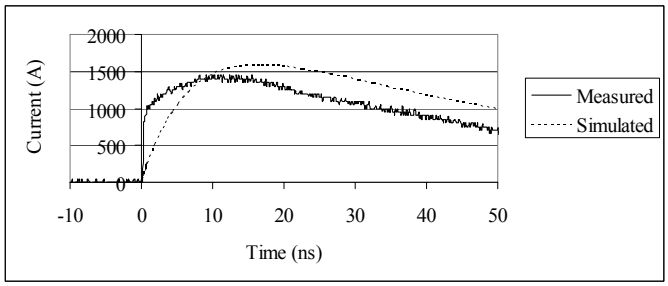

Fig. 7. Murata 0.47 µF, 250 V measured and simulated current.

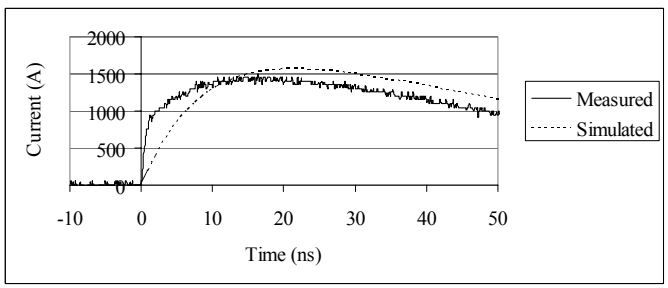

Fig. 8. Novacap 0.56 µF, 250 V measured and simulated current.

Table 1 Summary of capacitor parameters.

Vendor	Capacitance	Rated Voltage	Measured Ipeak	Measured TIpeak	Calculated R	Capacitor R	Capacitor L	Calculated Energy	Calculated Pmax into Matched Load	Package	Volume	Energy Density	Pmax Density
	(uF)	(V)	(A)	(ns)	(Ohms)	(Ohms	(nH)	(mJ)	(kW)		(cm^3)	(mJ/cm^3	(kW/cm^3)
Murata	0.1	1000	4140	4.5	0.18	0.16	0.40	50.0	2813	2220	0.0505	991	55739
AVX	0.1	1000	4400	7.4	0.17	0.15	0.62	50.0	2990	3630	0.2478	202	12067
Johanson	0.47	500	2880	7.5	0.13	0.11	0.48	58.8	979	2420	0.0787	747	12440
Vishay	0.33	500	3120	11.1	0.12	0.10	0.65	41.3	1060	2225	0.0721	572	14702
Murata	0.47	250	1410	12.4	0.13	0.11	0.81	14.7	240	1812	0.0248	593	9668
Novacap	0.56	250	1440	17.1	0.13	0.11	1.09	17.5	245	2225	0.0631	277	3877

Accuracy of the model tends to increase for the lower capacitance, higher voltage devices. This is potentially attributed to the transmission line behavior of MLC capacitors due to their fabrication geometry. Continued SMT capacitor study will address this observed effect.

Power and energy density calculations are included in Table 1. Energy is calculated from the rated capacitance and voltage. Peak power is calculated assuming the capacitor is discharging into a resistive load that matches the resistance of the capacitor.

VI. Conclusions

This paper presents the pulse discharge characteristics of a representative sample of SMT capacitors tested in the 0.1 to 0.5 µF, 250 to 1000 V range. This work in progress will continue to both evaluate capacitors and increase the accuracy of the Spice model.

Standard SMT capacitors can be successfully used in pulse discharge applications for many shots. However, their performance greatly varies between package styles and vendors. For example, in Table 1, the power and energy densities vary by a factor of 5 between the capacitors shown. Also, a comparison of the 250 V capacitors shows that they delivered a similar output even though one has less capacitance and a third of the package size.

Extensive Spice models do not exist for high voltage, high capacitance surface mount capacitors because they are typically used in bypass and filter circuits. Techniques have been published which quantify the parasitic inductance and resistance with measurements that rely solely on the wave shape, with the diagnostic influence factored out [2].

Table 2 Comparison of measured and simulated waveforms

Vendor	Capacitance (uF)	Measured Ipeak (A)	Measured TIpeak (ns)	Simulated Ipeak (A)	Simulated TIpeak (ns)	% Error Ipeak	% Error TIpeak
Murata	0.1	4140	4.5	4480	5.4	8.2	20.0
AVX	0.1	4400	7.4	4440	7.5	0.9	1.4
Johanson	0.47	2880	7.5	3250	13.6	12.8	81.3
Vishay	0.33	3120	11.1	3320	12.5	6.4	12.6
Murata	0.47	1410	12.4	1590	16.9	12.8	36.3
Novacap	0.56	1440	17.1	1570	22.5	9.0	31.6

However, these methods assume that the capacitor value remains constant during the discharge cycle, and that the output will oscillate through zero for low load impedances. For this reason, these methods are not applicable for this ceramic capacitor study due to the nonlinearities of the dielectric, though they work well for other types of capacitors.

Therefore, a first-pass LRC circuit model has been developed which reasonably predicts the peak current of actual measurements to within approximately 15% of their measured values, which is the critical parameter of this study. The time of peak current and the wave shape of the rising edge of the pulse are predicted less accurately. However, this simple model facilitates quickly evaluating many capacitors to select the best candidates for more detailed analysis.

A wide range of SMT capacitors have been tested for their ability to be employed in pulse discharge applications. The results have been presented here for a representative sample of capacitors. Clearly, their performance varies significantly and is not necessarily related to package size. Future directions include employing SMT devices in pulse discharge circuits for specific applications and continued model development.

VII. References

[1] Ness Engineering website http://home.san.rr.com/nessengr/techdata/rlc/rlc.html

[2] William C. Nunnally, M. Kristiansen, and Marion Hagler, "Differential Measurement of fast energy discharge capacitor, inductance, and resistance", *IEEE Transactions on Instrumentation and Measurement*, **24**, 2, 1975, pp. 112-114.

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